DLD-Project

Proposed-Solution

Roll No:

**19L-1127 & 19L-1135**

Project Name:

**4-bit Processer**

Group No:

**Group#1**

Circuits:

*Combinational circuits:-*

Decoders, Logic Gates, Sub-circuits for arithmetic operations.

*Sequential circuits:-*

Latches, Flip-flops, Clock pulse

Description:

Input:

First we’ll use 7 binary switches for instruction code. Then we’ll provide the first three bits to a 3x8 decoder and map all instructions to their respective subcircuits.

Processing:

The other four instruction bits will be stored in I and A data registers and will be provided to the subcircuits. The subcircuits will be made up of logic gates. The subcircuits will perform all the required operations as instructed by the instruction bits.

Output:

The outputs of subcircuits will be attached to registers. We’ll use latches with flip flops and clock pulses to preserve output. Clock pulse will be used for synchronization. The outputs of the subcircuits will be ANDed and then provided to the R1 and R2 data registers.